Senior logical Synthesis Engineer (M/F)

Context :

SiPearl is the company that is bringing to life the European Processor Initiative (EPI) consortium project, designing the high-performance, low-power microprocessor for the European exascale supercomputer. This new generation of microprocessors will help ensure Europe's technological sovereignty on the strategic markets for high performance computing, artificial intelligence and connected mobility.
By notably equipping the future European exascale supercomputer, SiPearl' s solutions will help drive the development of the European market for high performance computing (HPC), as well as its strategic applications such as artificial intelligence, Edge, and connected mobility.

Fluent in English to consolidate our growth and be part of the one, the newest and hottest tech adventure in Europe. SiPearl is looking for one Senior logical Synthesis Engineer.

Job opportunity in **Variable available (Germany, Spain?, France ?)**

Reporting to the implementation team manager, you will oversee this:

- Perform logical synthesis and create SDC and UPF constraints on multi-language RTL
- Work with RTL team to sort out RTL issues, suggesting solutions
- Insert Clock-Gating structures (manually and by use of tool) to improve dynamic power consumption
- Insert and verify Power-Aware structures, e.g. isolation, always-on-buffer (using UPF flow)
- Insert and verify DfT (Scan-Chain stitching, SpyGlass DfT, Mentor tooling)
- Bring-up and pipe-clean physical aware synthesis
- Deliver timing-clean synthesis module to PnR team
- Contribute in bring-up of Synthesis Flow (using Lynx environment)
- Work with IP design teams locally or remotely
- Work with ASIC service company for chip implementation in different time-zones

Qualifications and skills required

You are or you have:

- At least 5 years of experience of logical synthesis, constraint development and signoff
- Senior experience in using Synospys DC-NXT and Fusion-Compiler
- Senior experience in using STA tooling, especially Prime-Time
- Solid experience in RTL chip integration, including RTL design, integration and verification
- Experience in using Mentor-DfT tooling
- Experience in using power-aware techniques by use of UPF and VC LP
- Experience in LYNX environment
- Experience in GIT environment
- Good scripting skills, e.g. using TCL/Perl/Phyton
- Cadence tooling is a plus

Profile:

- Good problem-solving capability
- Good sense of independence and patient to learn and search technical information
- Good sense of flexibility and adaptation capability/sense of initiative
- Excellent oral and writing English communication

You are motivated by an experience within an industrial startup with fast growth and high visibility, having access to top notch silicon technology (beyond 7nm), all under a very competitive international environment. Send Resume and cover letter to cv@sipearl.com and please mention the job reference: #xxxxxx. After considering your application, we will call you to arrange a first interview. Our recruitment process consists of tests and about 3 interviews.