

Racyics

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DFT Engineer (Entry-Level)

Extending our international team, we are looking for a Design for Test (DFT) Engineer (Entry-Level).

Job description

- Implement and verify testability features to our System-on-Chip designs
- Create and simulate test patterns for production testing
- Develop DFT specifications and drive flow and methodology enhancements
- Implement and validate DFT structures such as JTAG, IJTAG, Scan & compression, IEEE1500, LBIST, MBIST, IP tests
- Take over full responsibility for tasks assigned to you

Requirements

- Bachelor's/Master's Degree in Electrical Engineering, Information Technology or similar required
- 0-2 years' experience in the Semiconductor industry
- Good understanding of digital logic and microelectronics
- Good programming skills (TCL is a plus)
- Experience with Design for Test concepts, hardware description languages as VHDL or Verilog and simulation of digital designs is a plus
- Self-driven and hands-on way of working
- Good written and oral communication skills in English
- Team-player

Location: Dresden or Frankfurt/Main (Neu-Isenburg)

Send us a mail with your CV incl. your certificates, transcripts etc. attached to jobs@racyics.com. Please mind that we can only consider attachments in PDF format.

About Us

Racyics® is Europe's leading design service provider for mixed-signal system-on-chip design and turnkey services in advanced nodes.

We deliver professional analog, digital and mixed-signal design services tailored to the customers' needs with focus on realization of complex System-on-Chips in leading edge technology nodes. Our team of more than 100 employees covers the complete chip design process up to system architecture development. Racyics is working for major German and international semi-custom companies both as a service provider and in collaborative partnerships.

Working at Racyics comes with many benefits, including flexible working hours, mobile work, a financial contribution to your childcare costs and great team events.